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Appin. No. 10/532,894

Attorney Docket No. 10808-235

Language Control

- Amendments to the Claims
 - (Cancelled).
- 2. (Previously Presented): A method for fabricating a transistor structure comprising at least a first and a second bipolar transistor having different collector widths, the method comprising:
 - A) providing a semiconductor substrate, and
- B) producing at least a first collector region of the first bipolar transistor having a first collector width and a second collector region of the second bipolar transistor having a second collector width,

wherein

- a) at least a first zone of a first buried layer of a first conductivity type of the first bipolar transistor and a first zone of a second buried layer of a first or a second conductivity type of the second bipolar transistor are introduced into the semiconductor substrate,
- b) a first epitaxial layer is produced, which covers, over the whole area, at least the first zones,
- c) at least a second zone of the first conductivity type is produced within the first epitaxial layer, the second zone adjoining the first zone of the first buried layer,
- d) a second epitaxial layer is produced, which covers, over the whole area, at least the first epitaxial layer and the second zone of the first buried layer,
- d) at least one insulation region is produced which isolates at least the collector regions from one another, and



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e) the second zone of the first buried layer adjoins the first collector region and the first zone of the second buried layer adjoins the second collector region.

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- 3-5. (Cancelled).
- 6. (Currently Amended): The method as claimed in claim 1, A method for fabricating a transistor structure comprising at least a first and a second bipolar transistor having different collector widths, the method comprising:

A) providing a semiconductor substrate,

- B) introducing at least a first buried layer of the first bipolar transistor and a second buried layer of the second bipolar transistor into the semiconductor substrate, and
- C) producing at least a first collector region having a first collector width on the first buried layer and a second collector region having a second collector width on the second buried layer.

<u>wherein</u>

- a) for the production of the second collector width, a first collector zone having a first thickness is produced on the second buried layer.
- b) a second collector zone having a second thickness is produced on the first collector zone.
- c) at least one insulation region is produced which isolates at least the collector regions from one another; and



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wherein an insulating layer is produced between the semiconductor substrate and the buried layers.

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7. (Currently Amended): The method as claimed in claim 1, A method for fabricating a transistor structure comprising at least a first and a second bipolar transistor having different collector widths, the method comprising:

A) providing a semiconductor substrate,

B) introducing at least a first buried layer of the first bipolar transistor and a second buried layer of the second bipolar transistor into the semiconductor substrate, and

C) producing at least a first collector region having a first collector width on the first buried layer and a second collector region having a second collector width on the second buried layer,

<u>wherein</u>

- a) for the production of the second collector width, a first collector zone having a first thickness is produced on the second buried layer,
- b) a second collector zone having a second thickness is produced on the first collector zone.
- c) at least one insulation region is produced which isolates at least the collector regions from one another; and

wherein the insulation region is produced with the aid of shallow trench isolation technology.

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- 8. (Previously Presented): The method as claimed in claim 2, wherein the second collector zone is deposited.
- 9. (Previously Presented): The method as claimed in claim 8, wherein the second collector zone is deposited epitaxially.
- 10. (Previously Presented): The method as claimed in claim 2, wherein an insulating layer is produced between the semiconductor substrate and the buried layers.
- 11. (Previously Presented): The method as claimed in claim 2, wherein the insulation region is produced with the aid of shallow trench isolation technology.

12-15. (Cancelled).

